CLAIMS

1. A process comprising:

forming a first recess in a substrate;

forming a conductive structure in the first recess;

first wet etching to expose a first portion of the conductive structure;

first rinsing the conductive structure; and

second non-wet etching to expose a second portion of the conductive structure.

2. The process of claim 1, wherein first wet etching includes first etching a polysilicon sacrificial second film that is disposed over the substrate.

3. The process of claim 1, and wherein first wet etching is at a rate that is faster than second non-wet etching.

4. The process of claim 1, wherein first wet etching is selected from a wet process and a vapor process, and wherein second non-wet etching is selected from a vapor process and a dry process.

5. The process of claim 1, wherein the substrate includes a single dielectric stack, wherein first wet etching is selected from a wet process and a vapor process, wherein second non-wet etching is selected from a vapor process and a dry process, and wherein the single dielectric stack is selected from undoped spin-on dielectric, undoped vapor-deposited dielectric, doped spin-on dielectric, and doped vapor-deposited dielectric.

6. The process of claim 1, wherein the substrate includes a single dielectric stack, wherein first wet etching is selected from a wet process and a vapor process, wherein second non-wet etching is selected from a vapor process and a dry process,

and wherein the single dielectric stack is selected from spin-on undoped silica, spin-on doped silica, borophospho silicate glass, borosilicate glass, phospho silicate glass, doped oxide from the decomposition of tetraethyl ortho silicate, and undoped oxide from the decomposition of tetraethyl ortho silicate.

7. The process of claim 1, wherein first wet etching includes a first etch chemistry, wherein second non-wet etching includes a second etch chemistry.

8. The process of claim 1, wherein forming a first recess includes forming the recess in a dielectric first film that is disposed above the substrate, and in a sacrificial second film that is disposed above and on the dielectric first film.

9. A process comprising:

forming a first recess in a substrate and wherein the first recess penetrates a dielectric first film that is disposed above the substrate and a sacrificial second film that is disposed above and on the dielectric first film;

forming a conductive structure in the first recess;

first etching to expose a first portion of the conductive structure, wherein first etching includes a first etch chemistry;

rinsing the conductive structure; and

second etching to expose a second portion of the conductive structure, wherein second etching includes a second etch chemistry.

10. The process of claim 9, wherein first etching includes plasma etching of the sacrificial film, wherein the sacrificial film includes polysilicon selected from undoped polysilicon, and heavily doped polysilicon.

11. The process of claim 9, wherein first etching includes first etching the sacrificial second film, and wherein second etching includes second etching the dielectric first film, wherein the dielectric first film is selected from an undoped dielectric, a doped dielectric, a spin-on deposited dielectric, a vapor-deposited

dielectric, an undoped polysilicon, a doped polysilicon, and combinations thereof, and wherein the sacrificial second film includes an undoped oxide.

12. The process of claim 9, wherein first etching removes the dielectric first film at a rate that is faster than second etching removes the sacrificial second film.

13. The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is vapor deposited.

14. The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is spin-on deposited.

15. The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is spin-on processed, and wherein the sacrificial second film is spin-on processed.

16. The process of claim 9, wherein the dielectric first film includes an undoped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is vapor deposited.

17. The process of claim 9, wherein the dielectric first film includes an undoped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is, and wherein the sacrificial second film is spin-on deposited.

18. The process of claim 9, wherein the dielectric first film includes an undoped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is spin-on deposited, and wherein the sacrificial second film is spin-on deposited.

19. The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes a doped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is vapor deposited.

20. The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes a doped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is spin-on deposited.

21. The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes a doped oxide, wherein the dielectric first film is spin-on deposited, and wherein the sacrificial second film is spin-on deposited.

22. A process comprising:

first etching a sacrificial second film to expose a first portion of a conductive structure, wherein first etching includes a first etch chemistry, and wherein first etching includes a first etch rate;

rinsing the conductive structure; and

second etching an amorphous carbon first film to expose a second portion of the conductive structure, wherein second etching includes a second etch chemistry, and wherein second etching includes a second etch rate that is slower than the first etch rate.

23. The process of claim 22, and wherein first etching removes the sacrificial second film at a rate that is faster than second etching removes the amorphous carbon first film.

24. The process of claim 22, wherein the sacrificial second film includes a doped oxide, and wherein the sacrificial second film is vapor deposited.

25. The process of claim 22, wherein the sacrificial second film includes a doped oxide, and wherein the sacrificial second film is spin-on processed.

26. The process of claim 22, wherein the sacrificial second film includes an undoped oxide, and wherein the sacrificial second film is vapor deposited.

27. The process of claim 22, wherein the sacrificial second film includes an undoped oxide, and wherein the sacrificial second film is spin-on processed.

28. The process of claim 22, wherein the sacrificial second film is selected from an oxide and a polysilicon, wherein first etching is selected from wet etching and vapor etching, and wherein second etching includes oxygen plasma stripping.

29. A process comprising:

first etching a sacrificial second film to expose a first portion of a conductive structure, wherein first etching includes a first etch chemistry;

first rinsing the conductive structure; and

second etching a dielectric first film, which is disposed below the sacrificial second film, to expose a second portion of the conductive structure, wherein second etching includes a second etch chemistry, and wherein first etching removes the sacrificial second film at a rate that is faster than second etching removes the dielectric first film.

30. The process of claim 29, wherein the dielectric first film includes an undoped oxide, and wherein first etching the sacrificial second film includes etching an undoped oxide.

31. The process of claim 29, wherein the dielectric first film includes an undoped oxide, and wherein first etching the sacrificial second film includes etching a doped oxide.

32. The process of claim 29, wherein the dielectric first film includes a doped oxide, and wherein first etching the sacrificial second film includes etching a doped oxide.

33. The process of claim 29, wherein the dielectric first film includes a doped oxide, and wherein first etching the sacrificial second film includes etching an undoped oxide.

34. The process of claim 29, wherein the dielectric first film includes an undoped oxide, and wherein first etching the sacrificial second film includes etching a doped polysilicon.

35. The process of claim 29, wherein the dielectric first film includes an undoped oxide, and wherein first etching the sacrificial second film includes etching an undoped polysilicon.

36. The process of claim 29, wherein the dielectric first film includes a doped oxide, and wherein first etching the sacrificial second film includes etching a doped polysilicon.

37. The process of claim 29, wherein the dielectric first film includes a doped oxide, and wherein first etching the sacrificial second film includes etching an undoped polysilicon.

38. The process of claim 29, wherein the dielectric first film includes an undoped polysilicon, and wherein first etching the sacrificial second film includes etching a doped polysilicon.

39. The process of claim 29, wherein the dielectric first film includes a lightly doped polysilicon, and wherein first etching the sacrificial second film includes etching a heavier-doped polysilicon.

40. A process comprising:

stripping amorphous carbon from conductive structure embedded therein, wherein the conductive structure is coupled to a substrate active area, and wherein the conductive structure includes an aspect ratio from about 6:1 to about 25:1.

41. The process of claim 40, wherein the conductive structure includes a container capacitor, and wherein stripping includes oxygen plasma stripping.

42. The process of claim 40, wherein the conductive structure is embedded in at least one additional sacrificial film, including a TEOS-decomposed sacrificial second film that is disposed above and on the amorphous carbon as a first film.

43. The process of claim 40, wherein the conductive structure is embedded in at least one additional sacrificial film, wherein the at least one additional sacrificial film includes a BPSG sacrificial second film disposed above and on the amorphous carbon as a first film.

44. The process of claim 40, wherein the conductive structure is embedded in at least one additional sacrificial film wherein the at least one additional sacrificial film includes an oxide sacrificial second film disposed above the amorphous carbon as a first film.

45. The process of claim 40, wherein the conductive structure is embedded in at least one additional sacrificial film wherein the at least one additional sacrificial film includes a polysilicon sacrificial second film disposed above the amorphous carbon as a first film.

46. A process comprising:

forming a recess in a first dielectric stack;

forming a conductive structure in the recess, wherein the conductive structure is partially embedded in the recess, and wherein the conductive structure is formed to extend from the first dielectric stack; and

electrically isolating the conductive structure.

47. The process of claim 46, the process further including:

forming a storage cell plate over the conductive structure.

48. The process of claim 46, wherein electrically isolating the conductive structure includes:

forming a storage cell dielectric film over the conductive structure.

49. The process of claim 46, the process further including:

forming a storage cell dielectric film over the conductive structure; and

forming a storage cell plate over the storage cell dielectric film.

50. The process of claim 46, wherein forming a storage cell dielectric film is carried out by chemical vapor deposition.

51. An intermediate system comprising:

a substrate;

a conductive structure electrically coupled to the substrate;

a dielectric first film into which the conductive structure is embedded;

a second etch fluid in contact with the dielectric first film, wherein the second etch fluid includes solution and reaction products of a second non-wet etch; and

a first etch fluid proximate the substrate, wherein the first etch fluid includes solution and reaction products of a wet-etch previously removed remnants of a sacrificial second film.

52. The intermediate system of claim 51, wherein the conductive structure includes a height-to width aspect ratio in a range from about 0.5:1 to about 25:1.

53. The intermediate system of claim 51, wherein the conductive structure is selected from polysilicon, a metal nitride, a metal carbide, a metal, a metal alloy, and a metal/metal nitride composite.

54. The intermediate system of claim 51, wherein the conductive structure is selected from a container capacitor and a stud capacitor.

55. An electrical device comprising:

a conductive structure electrically coupled to an active area, wherein the conductive structure is selected from a stud and a container, and wherein the conductive structure includes a height-to-width aspect ratio from greater than about 6:1 to about 25:1.

56. The electrical device according to claim 55, the electrical device further including:

a storage cell dielectric film disposed above the conductive structure; and

a storage cell plate disposed above the storage cell dielectric film.

57. The electrical device according to claim 55, wherein the conductive structure includes a height from about 0.5 micro meter to about 5 micro meter.

58. The electrical device according to claim 55, wherein the electrical device further includes:

a chip package, wherein the conductive structure is disposed in the chip package.

59. The electrical device according to claim 55, wherein the electrical device further includes:

a chip package, wherein the conductive structure is disposed in the chip package; and

a host, wherein the chip package is disposed in the host.

60. The electrical device according to claim 55, wherein the electrical device further includes:

a chip package, wherein the conductive structure is disposed in the chip package; and

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module.

61. The electrical device according to claim 55, wherein the electrical device further includes:

a chip package, wherein the conductive structure is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module; and

an electronic system, wherein the memory module is disposed in the electronic system.

62. The electrical device according to claim 55, wherein the electrical device further includes:

a chip package, wherein the conductive structure is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host includes a dynamic random access memory module; and

an electronic system, wherein the dynamic random access memory module is disposed in the electronic system.

63. The electrical device according to claim 55, wherein the electrical device further includes:

a chip package, wherein the conductive structure is disposed in the chip package;

a host, wherein the chip package is disposed in the host; and

an electronic system, wherein the host is disposed in the electronic system.

64. An electronic system, comprising:

a circuit module;

a user interface; and

a conductive structure disposed in the circuit module or the user interface, the conductive structure including:

a conductive structure electrically coupled to an active area, wherein the conductive structure is selected from a stud and a container, and wherein the conductive structure includes a height-to-width aspect ratio from greater than about 6:1 to about 25:1

65. The electronic system according to claim 64, wherein the user interface includes at least one of a keyboard, a pointing device, a monitor, a printer, a tuning dial, a display and speakers of a radio, an automobile ignition switch, an automobile gas pedal, a card reader, a keypad, and an automated teller machine.

66. The electronic system according to claim 64, wherein the circuit module includes a single integrated circuit.

67. A memory system, comprising:

a memory device;

a memory controller;

an external system bus;

a command link; and

a conductive structure disposed in the circuit module or the user interface, the conductive structure including:

a conductive structure electrically coupled to an active area, wherein the conductive structure is selected from a stud and a container, and wherein the conductive structure includes a height-to-width aspect ratio from greater than about 6:1 to about 25:1.

68. The memory system according to claim 67, wherein the memory system is selected from one of DIMM DRAM, a SIMM DRAM.

69. A computer system, comprising:

a processor;

a memory system coupled to the processor;

an input/output (I/O) circuit coupled to the processor and the memory system; and

a conductive structure disposed in the processor or the memory system, the conductive structure including:

a conductive structure electrically coupled to an active area, wherein the conductive structure is selected from a stud and a container, and wherein the conductive structure includes a height-to-width aspect ratio from greater than about 6:1 to about 25:1

70. The computer system according to claim 69, wherein the processor is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and a hand-held.

71. The computer system according to claim 69, wherein the memory system is selected from a DIMM DRAM, a SIMM DRAM, and wherein the computer system is selected from a personal computer, a server, and a network computer.